

METHODS OF AND APPARATUS FOR MANUFACTURING BALL GRID ARRAY  
SEMICONDUCTOR DEVICE PACKAGES

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BACKGROUND OF THE INVENTION

5 1. Field of the Invention

[0001] The present invention relates generally to the field of semiconductor device packaging. More specifically, the invention relates to methods of manufacturing ball grid array semiconductor packages for the packaging of semiconductor devices.

2. Description of Related Art

10 [0002] Some known methods of packaging semiconductor devices, such as semiconductor dies, integrated circuit chips, and the like, may include dual in-line packaging, pin grid array packaging, tape carrier packaging, and quad flat packaging. Nevertheless, as a pin count of a semiconductor device increases, the complexity of manufacturing semiconductor device packages using these known methods also may  
15 increase. Employing ball grid arrays semiconductor packages in order to package semiconductor devices may reduce the complexity of manufacturing semiconductor device packages because the ball grid array may serve as an electrical contact between the semiconductor package and an external component, such as a motherboard of a computer. Some known ball grid array packaging methods may include etching a  
20 conductor pattern onto either a first surface or a second surface of a substrate, and providing a plurality of conductive bump contact areas on the first surface of the substrate. With these known methods, a conductive bump, such as a semi-spherical or a substantial spherical solder bump, subsequently may be disposed on each of the conductive bump contact areas, and a semiconductor die may be mounted on or attached  
25 to the second surface of the substrate. Moreover, the conductive bumps may be electrically connected to the conductor pattern, such as by any known reflow process, which also may mechanically affix the conductive bumps to the first surface of the substrate. Nevertheless, if the conductive bump contact areas are not substantially aligned with their corresponding conductive bump before the conductive bumps are  
30 disposed on the first surface of the substrate, a sufficient electrical connection between the conductive bumps and the conductive bump contact areas may not be achieved.

Moreover, if the conductive bumps are of a non-uniform height, it may be more difficult to mount the conductive bumps to an external component, such as a motherboard of a computer, than if the conductive bumps were of a uniform height. Moreover, when the height of the conductive bumps are non-uniform, an electrical connection between the  
5 some of the conductive bumps and the external component may be weakened.

SUMMARY OF THE INVENTION

[0003] Therefore, a need has arisen for methods of manufacturing a ball grid array package which may overcome these and other shortcomings of the related art. A technical advantage of the present invention is that a conductive contact area of a  
10 substrate may be substantially aligned with a conductive bump before the conductive bump is disposed on the conductive contact area. Another technical advantage of the present invention is that the conductive bumps may have a substantially uniform height.

[0004] According to an embodiment of the present invention, a method for manufacturing a ball grid array semiconductor package is described. The method  
15 comprises the step of providing a substrate having a first surface and a second surface, in which the first surface or the second surface comprises a conductor pattern. The method also comprises the steps of providing a plurality of conductive bump contact areas on the first surface of the substrate, and substantially aligning each of the conductive bump contact areas with at least one conductive bump. The method further comprises the step  
20 of disposing at least one of the conductor bumps on each of the conductive bump contact areas. Moreover, the step of substantially aligning the conductive bump contact areas with at least one of the conductive bumps comprises the step of vibrating at least a portion of the substrate, which substantially aligns each of the conductive bump contact areas with at least one of said conductive bumps.

[0005] According to another embodiment of the present invention, an alignment  
25 apparatus is described. The alignment apparatus comprises means for pushing a film, e.g., a plurality of pushers, in which the film comprises at least one ball grid array semiconductor package. The ball grid array semiconductor package comprises a substrate having a plurality of conductive bump contact areas disposed on a first surface  
30 of the substrate. The apparatus further comprises means for vibrating the film, e.g., a plurality of vibrators, such as ultrasonic vibrators, contacting the pushing means, and the

vibration of the film substantially aligns each of conductive bump contact areas with at least one conductive bump positioned above the conductive bump contact areas.

[0006] Other features and advantages will be apparent to persons of ordinary skill in the art in view of the following detailed description of the invention and the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0007] For a more complete understanding of the present invention, needs satisfied thereby, and features and advantages thereof, reference now is made to the following descriptions taken in connection with the accompanying drawings.

10 [0008] **Fig. 1** is an exterior oblique view ball grid array semiconductor package according to an embodiment of the present invention.

[0009] **Fig. 2a-2b** are alignment apparatus for manufacturing a ball grid array package according to an embodiment of the present invention.

15 [0010] **Figs. 3** is a planarizing apparatus for manufacturing a ball grid array package according to an embodiment of the present invention.

[0011] **Fig. 4** is a flow chart of a method of manufacturing a ball grid array according to an embodiment of the present invention.

[0012] **Fig. 5** is a flow chart of a method of manufacturing a ball grid array according to an embodiment of the present invention.

20 [0013] **Fig. 6** is a flow chart of a method of manufacturing a ball grid array according to an embodiment of the present invention.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

25 [0014] Preferred embodiments of the present invention and their advantages may be understood by referring to **Figs. 1-6**, like numerals being used for like corresponding parts in the various drawings.

[0015] Referring to **Fig. 1**, a ball grid array semiconductor package 100 is described. Ball grid array semiconductor package 100 may comprise a substrate 103, such as an insulating substrate. For example, substrate 103 may be a film manufactured from a straight-chain non-thermoplastic polyimide. Moreover, substrate 103 may have a first surface 103b, which may be a bottom portion of substrate 103, and a second surface 103a, which may be a top portion of substrate 103. Ball grid array semiconductor

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package 100 also may comprise a plurality of conductive bumps 107, which may be formed on conductive bump contact areas (not shown) formed on first surface 103b. Ball grid array semiconductor package 100 further may comprise a semiconductor die 102 mounted on or attached to second surface 103a, which may be sealed to substrate 103 by a molding resin 109. For example, semiconductor die 102 may be attached to second surface 103a by a die attaching material disposed on second surface 103a, such as an adhesive manufactured from a non-conductive epoxy resin, or the like.

[0016] In one embodiment, first surface 103b may comprise a conductor pattern 104, which may electrically connect semiconductor die 102 to conductive bumps 107 when conductive bumps 107 are electrically connected to conductor pattern 104 and mechanically affixed to first surface 103b by any known reflow process. For example, conductive 104 may be a copper pattern, and the copper pattern may be formed by bonding a copper foil on first surface 103b by means of an adhesive layer, followed by an etching away of the undesired portions of the copper foil. Alternatively, second surface 103a may comprise conductor pattern 104, which may be formed on second surface 103a by any of the above described methods for forming conductor pattern 104.

[0017] Referring to **Figs. 2a-2b**, an alignment apparatus 200 for manufacturing a ball grid array semiconductor package, such as a ball grid array semiconductor package 100, is described. Alignment apparatus 200 may comprise pushing means, such as a plurality of pushers 114, which may be positioned on opposite sides of a film 122, which may comprise a plurality of substrates 103. For example, substrates 103 may be positioned on film 122 such that a distance between each substrate 103 may be substantially equal. Moreover, the pushing means may move film 122 in a predetermined direction. Alignment apparatus 200 further may comprise at least one means for vibrating substrate 103, such as at least one vibrator 112, which may contact at least a portion of the pushing means and also may be positioned adjacent to a first end of film 122. In one embodiment, vibrator 122 may be an ultrasonic vibrator. Alternatively, the means for vibrating substrate 103 may comprise a first vibrator 112, a second vibrator 112, and a third vibrator 112, which may be positioned adjacent to the first end of film 122, a second end of film 122, and a third end of film 122, respectively. In one embodiment, first vibrator 112, second vibrator 112, and third vibrator 112 each may be

an ultrasonic vibrator. Alignment apparatus 200 further may comprise means for lifting film 122, such as at least one backup plate 116.

[0018] In operation, the pushing means may move film 122 and substrates 103 in the predetermined direction, such as towards a plurality of conductive bumps 107, which  
5 may be disposed above film 122. When substrates 103 are in an appropriate position relative to conductive bumps 107, the means for vibrating may vibrate film 122 and substrates 103. For example, when film 122 vibrates and the means for vibrating comprise first vibrator 112, second vibrator 112, and third vibrator 112 positioned adjacent to the first end of film 122, the second end of film 122, and the third end of film  
10 122, respectively, film 122 may move in a direction towards a fourth end of film 122, i.e., the end of film 122 without a vibrator 122 positioned adjacent to the end. In this embodiment, moving film 122 in a single direction may allow the conductive bump contact areas (not shown) formed on first surface 103b of substrate 103 to substantially align with a corresponding conductive bump 107. When each of the conductive bump  
15 contact areas are substantially aligned with at least one conductive bump 107, the vibration of film 122 and substrates 103 may discontinue. The means for lifting film 122 then may lift film 122 towards conductive bumps 107 disposed above film 122, such that the conductive bump contact areas may contact the corresponding conductive bump 107, which may dispose each conductive bump 107 on the corresponding conductive bump  
20 contact area.

[0019] Referring to **Fig. 3**, a planarizing apparatus 300 is described. Planarizing apparatus 300 may comprise means for holding a ball grid array semiconductor package, such as a ball grid array semiconductor package 100. For example, the means for holding ball grid array semiconductor package 100 may be a vacuum 118. Planarizing apparatus  
25 300 also include means for planarizing conductive bumps 107, which may be a planarizing surface 120. In operation, after conductive bumps 107 are disposed on the conductive bump contact areas formed on first surface 103b and are mechanically affixed to first surface 103b by any known reflow process, the means for holding ball grid array semiconductor package 100 may lower ball grid array semiconductor package 100 onto  
30 the means for planarizing conductive bumps 107, such that conductive bumps 107 may contact the means for planarizing conductive bumps 107 with a predetermined force. The

predetermined force may be a force sufficient to decrease a height of any non-uniform conductive bumps 107, such that a height of each conductive bump 107 may be substantially uniform relative to the height of each of the other conductive bumps 107.

[0020] Referring to **Fig. 4**, a method 400 for manufacturing a ball grid array semiconductor package, such as a ball grid array semiconductor package 100 according to any of the described embodiments of the present invention, is described. In step 402, a substrate 103, having a first surface 103b and a second surface 103a, may be provided. In one embodiment, first surface 103b may comprise a conductor pattern 104. Alternatively, second surface 103a may comprise conductor pattern 104. In step 404, a plurality of conductive bump contact areas (not shown) may be provided on first surface 103b. In step 406, each of the conductive bump contact areas may be substantially aligned with at least one conductive bump 107 by vibrating at least a portion of substrate 103. For example, at least a portion of substrate 103 may be ultrasonically vibrated. In one embodiment, a first end, a second end, and a third end of a film 122 may be vibrated or ultrasonically vibrated, which may substantially align each of the conductive bump contact areas with at least one corresponding conductive bump 107. In each of the above described embodiments, when each of the conductive bump contact areas are substantially aligned with at least one conductive bump 107, the vibration of at least a portion of substrate 103 may be discontinued. Moreover, in step 408, at least one conductive bump 107 may be disposed on each of the conductive bump contact areas.

[0021] Referring to **Fig. 5**, a method 500 for manufacturing a ball grid array semiconductor package, such as a ball grid array semiconductor package 100 according to any of the described embodiments of the present invention, is described. In step 502, a substrate 103, having a first surface 103b and a second surface 103a, may be provided. In one embodiment, first surface 103b may comprise a conductor pattern 104. Alternatively, second surface 103a may comprise conductor pattern 104. In step 504, a plurality of conductive bumps 107 may be disposed on first surface 103b. In step 506, a semiconductor die 102 may be mounted on or attached to second surface 103a. In step 508, conductive bumps 107 may be electrically connected to conductor pattern 104, such as by any known reflow process, which also may mechanically affix conductive bumps 107 to first surface 103b. In step 510, ball grid array semiconductor package 100 may be

mechanically tested, which may comprise determining whether a height of conductive bumps 107 are substantially uniform. In step 512, conductive bumps 107 may be planarized when the height of at least one conductive bump 107 is non-uniform relative to the height of at least one other conductive bump 107. For example, planarizing  
5 conductive bumps 107 may comprise the step of contacting conductive bumps 107 with a planarizing surface 120 with a predetermined amount of downward force. Moreover, the predetermined force may be a force sufficient to decrease a height of any non-uniform conductive bumps 107, such that a height of each conductive bump 107 may be substantially uniform relative to the height of each of the other conductive bumps 107.

10 [0022] Referring to **Fig. 6**, a method 600 for manufacturing a ball grid array semiconductor package, such as a ball grid array semiconductor package 100 according to any of the described embodiments of the present invention, is described. In step 602, a substrate 103, having a first surface 103b and a second surface 103a, may be provided. In one embodiment, first surface 103b may comprise a conductor pattern 104.  
15 Alternatively, second surface 103a may comprise conductor pattern 104. In step 604, a plurality of conductive bump contact areas (not shown) may be provided on first surface 103b. Moreover, in step 604, each of the conductive bump contact areas may be substantially aligned with at least one conductive bump 107 by vibrating at least a portion of substrate 103. For example, at least a portion of substrate 103 may be ultrasonically  
20 vibrated. In one embodiment, a first end, a second end, and a third end of a film 122 may be vibrated or ultrasonically vibrated, which may substantially align each of the conductive bump contact areas with at least one corresponding conductive bump 107. In each of the above described embodiments, when each of the conductive bump contact areas are substantially aligned with at least one conductive bump 107, the vibration of at  
25 least a portion of substrate 103 may be discontinued. In step 606, at least one conductive bump 107 may be disposed on each of the conductive bump contact areas. In step 608, a semiconductor die 102 may be mounted on or attached to second surface 103a. In step 610, conductive bumps 107 may be electrically connected to conductor pattern 104, such as by any known reflow process, which also may mechanically affix conductive bumps  
30 107 to first surface 103b. In step 612, ball grid array semiconductor package 100 may be mechanically tested, which may comprise determining whether a height of conductive

bumps 107 are substantially uniform. In step 614, conductive bumps 107 may be planarized when the height of at least one conductive bump 107 is non-uniform relative to the height of at least one other conductive bump 107. For example, planarizing conductive bumps 107 may comprise the step of contacting conductive bumps 107 with a planarizing surface 120 with a predetermined amount of downward force. Moreover, the predetermined force may be a force sufficient to decrease a height of any non-uniform conductive bumps 107, such that a height of each conductive bump 107 may be substantially uniform relative to the height of each of the other conductive bumps 107.

[0023] While the invention has been described in connection with preferred embodiments, it will be understood by those of ordinary skill in the art that other variations and modifications of the preferred embodiments described above may be made without departing from the scope of the invention. Other embodiments will be apparent to those of ordinary skill in the art from a consideration of the specification or practice of the invention disclosed herein. It is intended that the specification and the described examples are considered exemplary only, with the true scope and spirit of the invention indicated by the following claims.



## PATENT

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**Figure 1.** The effect of the number of iterations on the accuracy of the proposed algorithm. The figure shows two plots side-by-side. The left plot shows the error norm  $\|e\|_2$  versus the number of iterations  $n$ , ranging from 0 to 100. The right plot shows the relative error  $\frac{\|e\|_2}{\|x\|_2}$  versus the number of iterations  $n$ , ranging from 0 to 100. Both plots show a decreasing trend as the number of iterations increases, indicating convergence.